A Monolithic Si PCS–CDMA Power Amplifier With 30% PAE at 1.9 GHz Using a Novel Biasing Scheme

Sifen Luo, *Member, IEEE,* and Tirdad Sowlati, *Member, IEEE*

***Abstract*—A monolithic Si personal-communication-system–CDMA power amplifier (PA) capable of delivering 28.2-dBm output power with 30% power-added efficiency and −45-dBc adjacent-channel-power ratio at 1.9 GHz and 3.6-V supply voltage is presented for the first time in this paper. The PA implemented in a 30-GHz BiCMOS process incorporates a novel impedance-controllable biasing scheme to control the class of operation and bias impedance of the output stage. Both simulated and measured results are presented for comparison.**

***Index Terms*—BiCMOS analog integrated circuits, code-division multiple access, power amplifiers, radio-frequency amplifiers.**

I. Introduction

MONOLITHIC RF power amplifiers (PAs) for mobile-phone handset applications have traditionally been the territory of GaAs technologies. Efforts have been made on designing nonlinear PAs [1], [2] at both the cellular frequency (900 MHz) band and the personal-communication-system (PCS) frequency (1.9 GHz) band by using Si technologies. Recently, high-efficiency linear PAs were demonstrated at the above two bands by using SiGe heterojunction-bipolar-transistor (HBT) technologies [3], [4]. The PA for the code-division-multiple-access (CDMA) applications at the lower band could deliver 28-dBm output power with 36% power-added efficiency (PAE) and −44.1-dBc adjacent-channel-power ration (ACPR) [3], while the CDMA PA at the higher band could deliver 30-dBm output power with 41% PAE and −46-dBc ACPR [4]. However, the latter was still a hybrid solution. Si monolithic RF PAs have advantages in low cost and ease of integration with other mainstream Si-based circuits. To date, no monolithic Si PCS–CDMA PA has been reported yet.

The modulation scheme of the CDMA system requires the PA used in the handset to be highly linear. This makes it very challenging to design a monolithic PCS–CDMA PA with high efficiency using Si technologies due to their inherently high substrate loss and parasitics.

A monolithic Si PCS–CDMA PA capable of delivering 28.2-dBm output power with 30% PAE, −45-dBc ACPR, and 21.5–dB gain at 1.9 GHz and a supply voltage of 3.6 V is demonstrated for the first time in this paper. The PA was mounted chip-on-board (COB) with low-cost surface-mount components for both input and output matching networks. The results were obtained from an FR-4 test board by using a 50-Ω measurement system.

In Section II, a conventional biasing scheme for the output stage of the PA is discussed. An impedance-controllable biasing scheme for the PA and its advantages over the conventional one are then presented in Section III. Simulated and measured results of the PA with the impedance-controllable biasing scheme are given in Sections IV and V, respectively. Finally, a conclusion is drawn in Section VI.

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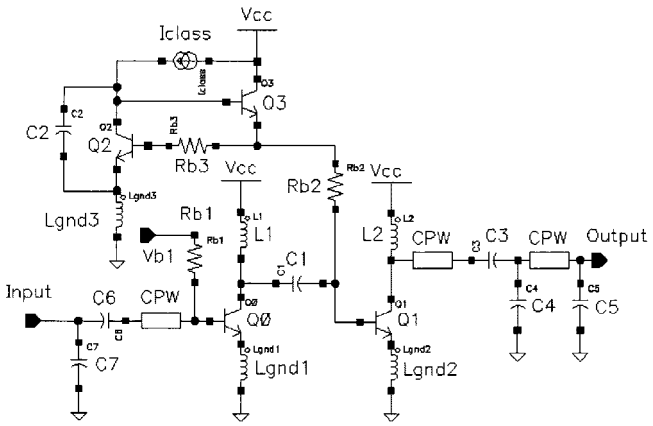

Fig. 1. Schematic of the PA with a conventional biasing scheme.

II. Conventional Biasing Scheme

Fig. 1 shows a simplified schematic of a PA consisting of two common-emitter stages ($Q0$ and $Q1$). The output-matching network consists of capacitors $C3$ to $C5$, inductors $L2$, and two transmission lines, i.e., coplanar waveguides (CPWs). The input matching network consists of capacitors $C6$ and $C7$ and a transmission line (i.e., CPW). The input stage is biased through an on-chip resistor R_{b1} by using a bias voltage V_{b1} for simplicity. A conventional current-mirror circuit comprised of $Q2$ and $Q3$ is used to bias the output stage.

In Fig. 1, $L_{\rm gnd1}$, $L_{\rm gnd2}$, and $L_{\rm gnd3}$ are ground inductors from bonding wires. $L1$ and $L2$ are off-chip inductors. The interstage-matching network consists of an on-chip capacitor $C1$ and $L1$ realized using a bonding wire and a printed-circuit-board (PCB) trace. $C2$ is an on-chip bypass capacitor.

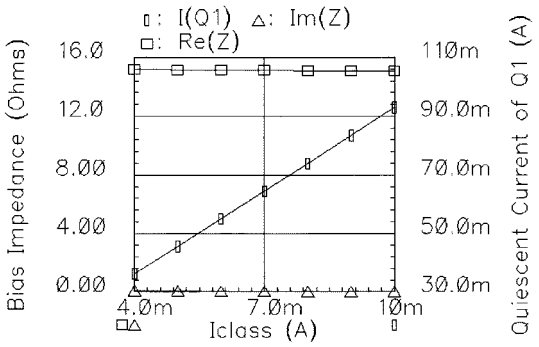

Fig. 2. Quiescent current of $Q1$ and small-signal impedance (1 MHz) of the conventional biasing scheme as functions of $I_{\rm class}$ ($R_{b2} = 15\ \Omega$).

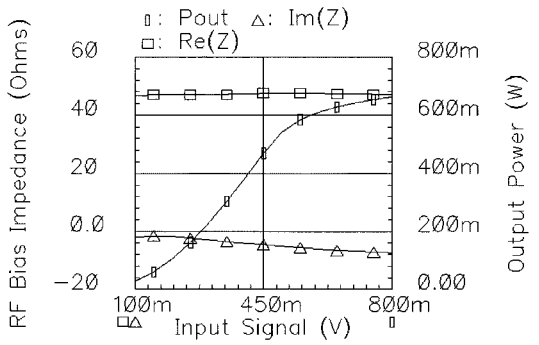

Fig. 3. RF impedance of the conventional biasing scheme and output power of the PA as functions of the input signal level ($R_{b2} = 15\ \Omega$, $I_{\rm class} = 8$ mA).

This biasing scheme for $Q1$ provides a near-constant small-signal impedance (1 MHz) presented at the base of $Q1$ and a nearly linear control of the collector's quiescent current of $Q1$, as shown in Fig. 2, with $R_{b2} = 15\ \Omega$. When $Q0$ and $Q1$ are biased into class-AB operation, however, its large-signal impedance presented at the base of $Q1$ at 1.9 GHz is capacitive and much larger than its small-signal counterpart, as shown in Fig. 3, where the PAs output power versus input signal levels is also shown. It is seen that the PA starts to saturate at the output power close to 600 mW. This is due to the fact that, as the output power increases, the average voltage drop across the bias impedance increases. This causes a reduction in the base–emitter voltage of $Q1$ and, thus, pushes it into saturation [5].

III. Impedance-Controllable Biasing Scheme

Fig. 4 shows a simplified schematic of a PA using an impedance-controllable biasing scheme to bias $Q1$ [6]. It is identical to the PA shown in Fig. 1, except for the biasing scheme for $Q1$. The biasing scheme is comprised of two current-mirror subcircuits: one consisting of transistors $Q2, Q4$, and $Q7$ and the other consisting of transistors $Q5$ and $Q6$. This biasing scheme is capable of providing independent control of bias impedance and class of operation of $Q1$ by properly choosing $I_{\rm class}$ and $I_{\rm bias}$. Whereas $I_{\rm bias}$ controls the output impedance of the bias circuit, $I_{\rm class}$ controls the quiescent current of the output stage. This proposed biasing scheme allows the output stage to be adjusted for optimum efficiency and linearity.

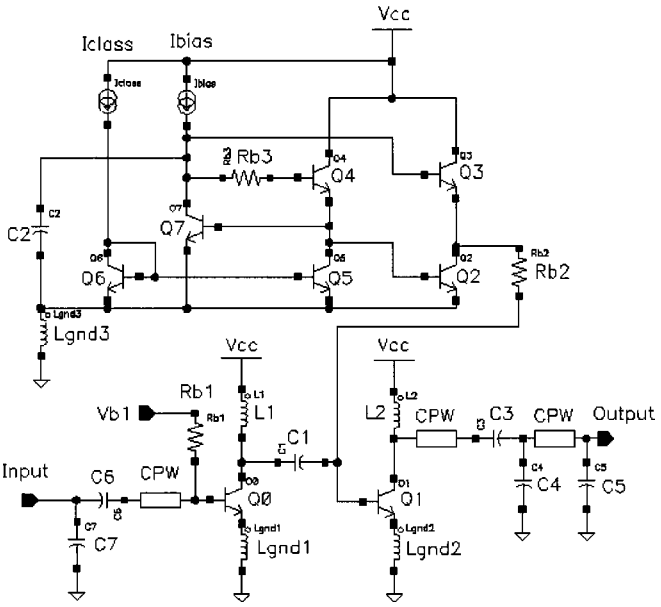

Fig. 4. Schematic of the PA with an impedance-controllable biasing scheme.

The mechanism of its controlling the quiescent current is explained as follows. Neglecting base currents, we have

$$V_{\rm be}(Q1) + V_{\rm be}(Q3) + V(R_{b2}) = V_{\rm be}(Q2) + V_{\rm be}(Q4) + V(R_{b3}) \quad (1)$$

and since $Q2$ and $Q3$ have the same current, we then have

$$V_{\rm be}(Q3) = V_{\rm be}(Q2). \quad (2)$$

This leads to

$$V_{\rm be}(Q1) = V_{\rm be}(Q4) \quad (3)$$

when

$$V(R_{b2}) = V(R_{b3}) \quad (4)$$

by properly choosing R_{b2} and R_{b3}. The current flowing in $Q6$ must flow in $Q5$ and $Q4$ because $Q5$ and $Q6$ form a current mirror. Since $I_{\rm class}$ controls the current flowing in $Q6$, it, therefore, dictates the quiescent current in $Q4$, which, in turn, controls the quiescent current in the output transistor $Q1$.

The mechanism of $I_{\rm bias}$'s controlling the output impedance of the biasing circuit can be explained in a similar fashion. Since $Q2, Q4,$, and $Q7$ form a current mirror, the current flowing in $Q2$ and $Q3$ is proportional to $I_{\rm bias}$ if we neglect the base currents. The quiescent current of $Q3$, which is controlled by $I_{\rm bias}$, determines the emitter resistance of $Q3$. The impedance of the biasing circuit for $Q1$ is the summation of R_{b2} and the impedance at the emitter of $Q3$. At the desired operating frequencies, the impedance presented at the base of $Q3$ is quite low due to the bypass capacitor $C2$. Hence, its reflected impedance at the emitter of $Q3$ is also very low. Therefore, $I_{\rm bias}$ controls the impedance of the biasing circuit for $Q1$. The effect of $I_{\rm bias}$ on the quiescent current of $Q1$ is much smaller than that of $I_{\rm class}$ (refer to Figs. 5 and 6).

By properly scaling the emitter area ratios between transistor pairs, one can readily control the quiescent current of the output

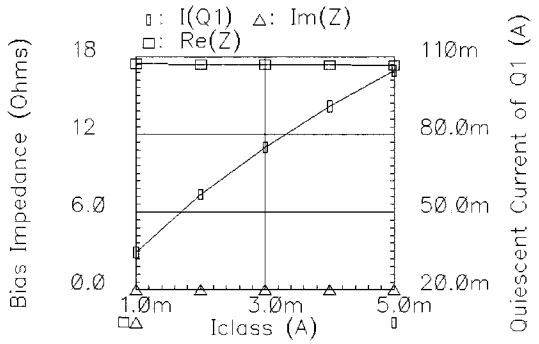

Fig. 5. Quiescent current of $Q1$ and small-signal impedance (1 MHz) of the impedance-controllable biasing scheme as functions of $I_{\rm class}$ ($R_{b2} = 15\ \Omega$, $I_{\rm bias} = 3$ mA).

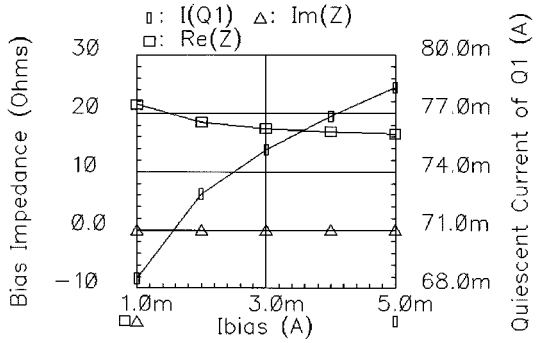

Fig. 6. Quiescent current of $Q1$ and small-signal impedance (1 MHz) of the impedance-controllable biasing scheme as functions of $I_{\rm bias}$ ($R_{b2} = 15\ \Omega$, $I_{\rm class} = 3$ mA).

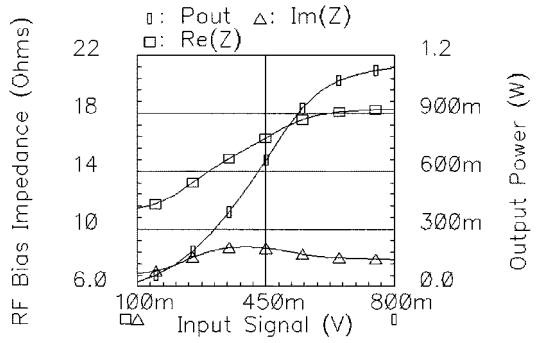

Fig. 7. RF impedance of the impedance-controllable biasing scheme and output power of the PA as functions of the input signal level ($R_{b2} = 15\ \Omega$, $I_{\rm class} = I_{\rm bias} = 3$ mA).

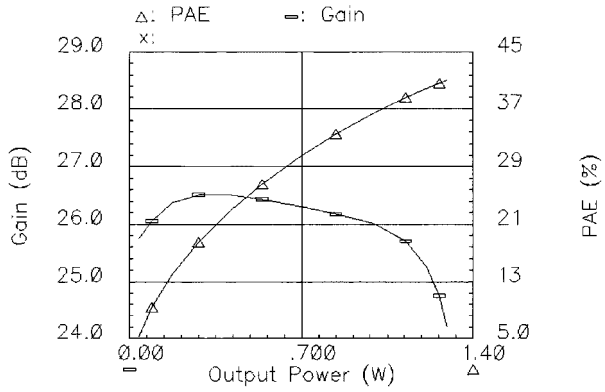

Fig. 8. Gain and PAE of the PA as functions of the output power ($V_{b1} = 0.88$ V, $R_{b2} = 15\ \Omega$, $I_{\rm class} = I_{\rm bias} = 3$ mA).

stage and the output impedance of the bias circuit. This helps to optimize the efficiency of the output stage, while maintaining the required linearity.

The collector's quiescent current of $Q1$ and low-frequency (1 MHz) small-signal impedance of the impedance-controllable biasing scheme presented at the base of the output stage as functions of $I_{\rm class}$ and $I_{\rm bias}$ are shown in Figs. 5 and 6. For simplicity, R_{b3} is set to zero ($R_{b3} = 0$) in this analysis. It is seen that the control current $I_{\rm class}$ in both biasing schemes has a similar effect on the quiescent current of $Q1$ and the bias impedance: near-constant bias impedance and nearly linear control of the quiescent current. Furthermore, the control current $I_{\rm bias}$ provides an additional means to adjust the bias impedance and only slightly changes the quiescent current.

It is of more interest to see its large-signal impedance presented at the base of $Q1$ at 1.9 GHz. Fig. 7 shows the RF impedance of the impedance-controllable biasing scheme and the output power as a function of the input signal level. For a fair comparison, the sizes of $Q0$ and $Q1$ and the bias conditions have been set identical to those for the PA discussed in Section II. There are several advantages of using the impedance-controllable biasing scheme. Firstly, it presents low impedance at the base of $Q1$. Secondly, its large-signal impedance is inductive and not far off from its low-frequency small-signal values. This helps interstage matching by canceling part of the capacitive base impedance of $Q1$. Thirdly, it helps increase output power due to its low RF impedance. As seen in Fig. 7, the PA only starts to saturate at the output power close to 1 W. This is a significant improvement over that of the PA with the conventional biasing scheme.

IV. Simulated Results

Although the output power of the CDMA PA with a digitally modulated input signal is measured differently than that of a PA with a continuous-wave (CW) input signal, the required maximum output power level (28 dBm or 631 mW) of the CDMA PA is still used as a reference in the PA design using Cadence's Spectre. The design methodology for the PA is as follows. Spectre is first used to achieve a relatively flat gain in a large range of the output power and PAE close to 30% at the reference power level by properly adjusting $I_{\rm class}$ and $I_{\rm bias}$. Agilent Technologies' Circuit Envelope Simulator is then used to simulate the PA's ACPRs.

Whereas the input of the PA shown in Fig. 4 was quite well matched to 50 Ω, the output of the PA was connected to a 50-Ω load through the output-matching network. The gain and PAE of the PA simulated in Spectre as functions of the output power are shown in Fig. 8. A peak gain of 26.5 dB appears at the output power of about 300 mW. The gain is quite flat over a large range of output power (from 100 mW to 1 W) with a variation of about 0.5 dB. At the reference power level (631 mW), its PAE is fairly close to 30%. The gain curve further indicates that the PA is still operated in a linear region at the reference output power level.

Since a handset has to be operable in an environment where the ambient temperature may range from −40 °C to 85 °C, it

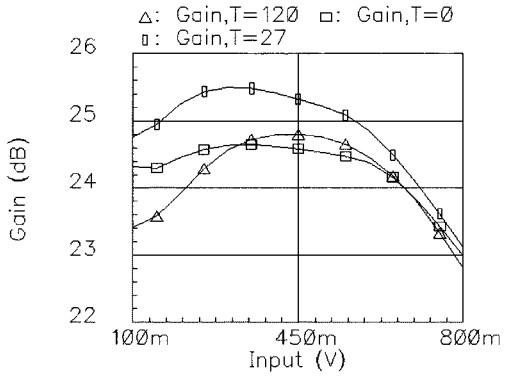

Fig. 9. Gain of the PA as a function of the input signal level with the junction temperature T in Celsius as a parameter ($V_{b1} = 0.88$ V, $R_{b2} = 15\ \Omega$, $I_{\rm class} = I_{\rm bias} = 3$ mA).

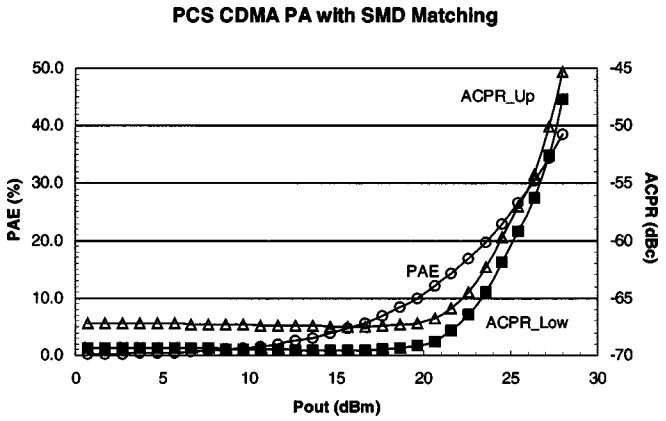

Fig. 10. Simulated ACPR and PAE of the PA.

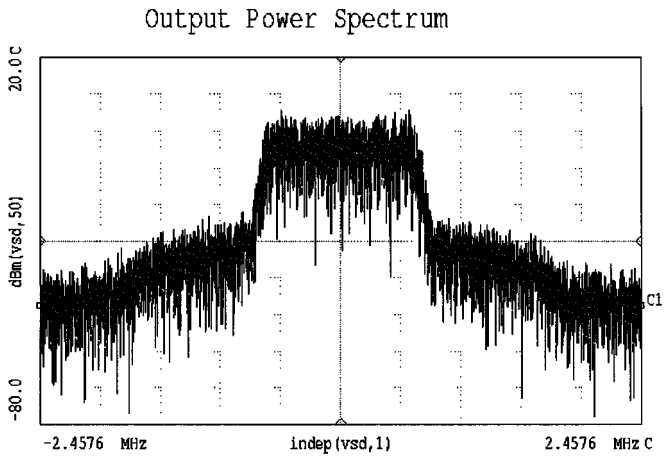

Fig. 11. Snapshot of the ACPR simulation at the output power of 28 dBm.

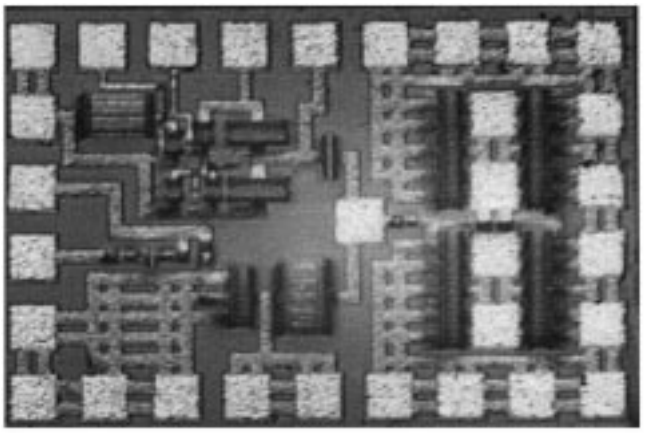

Fig. 12. Photomicrograph of the die.

is important for the PA to meet specifications within the temperature range. A change in the ambient temperature leads to a change in the junction temperature of transistors. The effect of transistor's junction temperature on the gain of the PA is shown in Fig. 9, where T stands for the junction temperature in Celsius. As the junction temperature changes from 0 °C to 120 °C, the maximum gain variation is about 1.4 dB, which occurs at the lowest input signal level as shown.

In the circuit envelope simulation, a CDMA input signal was used to simulate the PA's performance. The simulation results are shown in Fig. 10. At the required output power of 28 dBm, the PA achieves PAE of 38% and a gain of 22 dB with ACPRs less than -45 dBc. The ACPRs stay flat at lower power levels and then increase monotonically at higher power levels.

The higher PAE obtained from circuit envelope simulation than that obtained from Spectre is partly due to the fact that two different transistor models were used in the simulations. The Mextram model was used in Spectre simulation. However, we used the Gummel–Poon model in the circuit envelope simulation because the Mextram model had a convergence problem. The Mextram model predicts the behavior of the transistor more accurately. Simulated *I-V* characteristics of the two models indicate the Gummel–Poon model overestimates the output power capability and, hence, leads to overestimating the PAE.

Nevertheless, the impedance-controllable biasing scheme allowed the PA to achieve the required ACPR with efficiency higher than 30%. Fig. 11 shows the output spectrum of the PA with ACPR less than -45 dBc at the output power level of 28 dBm.

V. Measured Results

The PA with the impedance-controllable biasing scheme was implemented in a Philips BiCMOS process (QUBiC3) featuring 30-GHz ft NPNs, 0.5-μm CMOS, and high-value poly resistors. The emitter area of $Q1$ is 128 $\times$ 0.7 μm$\times$ 20.2 μm. A photomicrograph of the die with an area of about 0.9 mm^2 is shown in Fig. 12.

The PA was first tested at 1.9 GHz with a three-stub tuner in the output for benchmarking its performance. Both the input and output stages were biased in a class-AB operation. The PA's ACPR and PAE versus the output power are shown in Fig. 13. A spectrum analyzer from Rohde & Schwarz, Munich, Germany, was used in the ACPR measurements. With the output matched using the tuner, the PA delivers 28.1-dBm output power with 24.5-dB gain, 31.5% PAE and -45-dBc ACPR. It is worth noting that, in this PA, there is a valley with a quite steep slope in the ACPR curve. This indicates that one can improve ACPR margins with a slight backoff from the highest output power level.

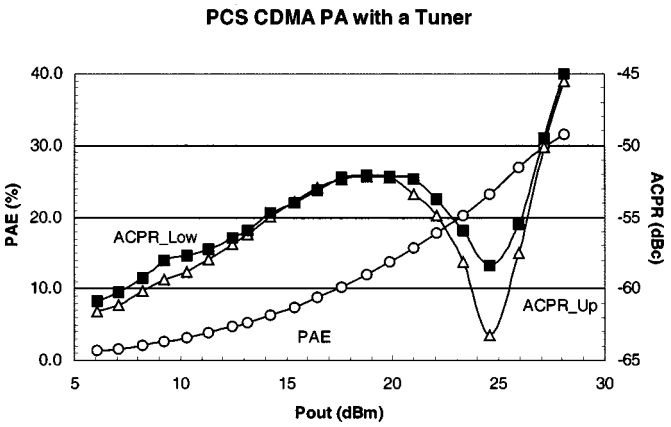

Fig. 13. Measured ACPR and PAE of the PA with the tuner.

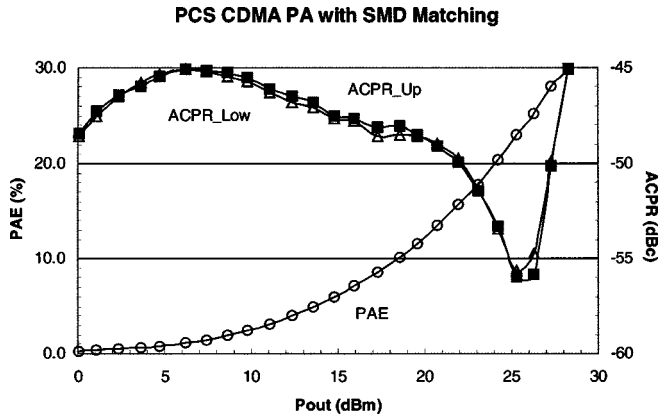

Fig. 14. Measured ACPR and PAE of the PA with matching networks using surface-mount components.

The tuner was then replaced by surface-mount components on the FR-4 test board. The PA was again tested at 1.9 GHz with a slightly lower base bias voltage for the input stage to enhance its PAE. I_{class} and I_{bias} were readjusted to compensate drops in PAE and gain due to the insertion loss from the surface-mount components. The PAs ACPR and PAE versus the output power are shown in Fig. 14. With the input and output matching networks using the low-cost surface-mount components on the FR-4 test board, the PA delivers 28.2-dBm output power with 21.5-dB gain, 30% PAE, and −45-dBc ACPR. The same steep slope can be seen in the ACPR curve near the peak output power level. At lower output power levels, there is a peak almost reaching the ACPR limit (−45 dBc) in the ACPR curve due to the lower bias in the input stage.

Compared with the simulated ACPR curves, one can readily notice that the measured ones are quite different from those simulated in both cases of the PA matched with the output tuner and surface-mount components. This is partly due to lower biases used in the measurements. A better understanding of this requires more simulations and measurements.

Fig. 15 shows an actual ACPR measurement of the PA matched with the surface-mount components at its highest linear output power level. A 10-dB attenuator and a coaxial cable were used in the output. Their combined measured attenuation is 10.8 dB. This attenuation plus the reading of 17.45-dBm channel power adds up to 28.25-dBm output power.

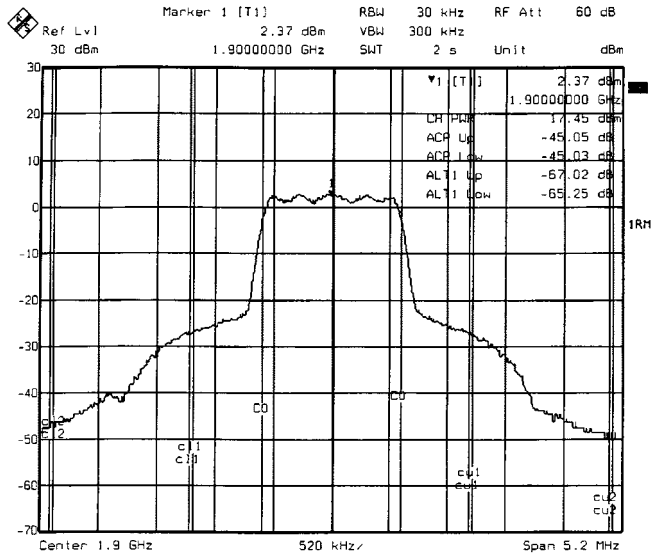

Fig. 15. Snapshot of the ACPR measurement of the PA with the matching networks using surface-mount components.

It is seen that whereas the ACPR reaches its specified limit of −45 dBc, the alternate-channel-power ratio has large margins over its specification of −56 dBc. The effectiveness of the impedance-controllable biasing scheme has been verified in these measurements.

Again, compared with the simulated output power spectrum shown in Fig. 11, the measured one shows much better alternative channel power ratios.

VI. Conclusion

In this paper, an Si PCS–CDMA PA with a novel impedance-controllable biasing scheme, mounted COB, and matched with low-cost surface-mount components has been demonstrated for the first time, which is capable of delivering 28.2-dBm output power with 30% PAE, −45-dBc ACPR, and 21.5-dB gain at 1.9 GHz and 3.6-V supply voltage.

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